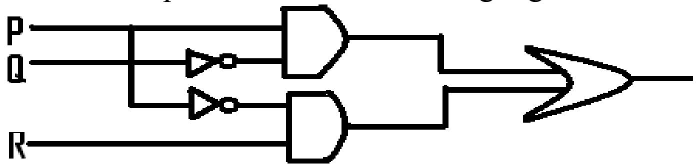
BOOLEAN ALGEBRA QUESTIONS

2009 Outside Delhi:

6. (a) State and verify absorption law using truth table. 2

(b) Write the equivalent Boolean Expression for the following logic circuit: 2



(c)Write the POS form of a Boolean function G, which is represented in a truth table as follows 1

U	V	W	G
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

(d) (d) Reduce the following Boolean expression using K-map: 3

H(U,V,W,Z) = ∑(0,1,4,5,6,7,11,12,13,14,15)

2008 Outside Delhi:

6. (a) State and Verify Absorption law in Boolean Algebra. 2

(b) Draw a logical circuit diagram for the following Boolean Expression: A.(B+C’) 1

(c) Convert the following Boolean expression into its equivalent Canonical Product of sum form (POS): A.B’C + A’.B.C + A’.B.C’. 2

(d) Reduce the following Boolean expression using K-map: 3

F(A,B,C,D) = ∑(0,1,2,,4,5,8,9,10,11)

2008 Delhi:

6. (a) State and verify De Morgan’s law in Boolean Algebra. 2

(b) Draw a Logical Circuit Diagram for the following Boolean Expression. X’.(Y’+Z) 1

(c) Convert the following Boolean expression into its equivalent Canonical Sum of Product Form (SOP): (X’+Y+Z’).(X’+Y+Z).(X’+Y’+Z).(X’+Y’+Z’) 2

(d) Reduce the following Boolean Expression using K-map. 3

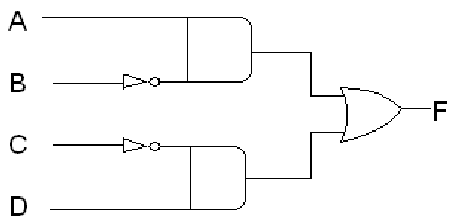
F(A,B,C,D) = ∑(0,2,3,4,6,7,8,10,12)

2007 Outside Delhi:

6. (a) State De Morgan’s Theorems and verify the same using truth table. 2

(b) Write the equivalent canonical product of sum expression for the following sum of product expression: **F(X, Y,Z) = ∑ (0, 2,4,5)** 2

(c) Write the equivalent Boolean expression for the following logic circuit 2



(d) Reduce the following Boolean expression using K – Map : 2

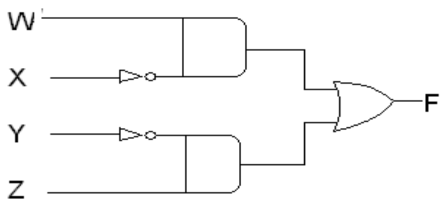
F(A, B, C, D,) = Π (5, 6, 7, 8, 9, 12, 13, 14, 15)

2007 Delhi:

6 (a) State Distributive law and verify the same using truth table. 2

(b) Write the equivalent canonical product of sum expression for the following sum of product expression: **F(X, Y,Z) = Π (1,3,6,7)** 2

(c) Write the equivalent Boolean expression for the following logic circuit 2



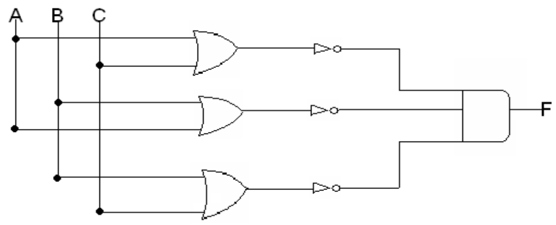
d) Reduce the following Boolean expression using K – Map : 2

F(U, V, W, Z) = ∑(0,1,2,3,4,10,11)

2006 Outside Delhi:

6. (a) State and verify Associative Law. 2

(b) Write the equivalent expression for the following Logic Circuit : 2



(c) Express P +Q'R in POS form. 1

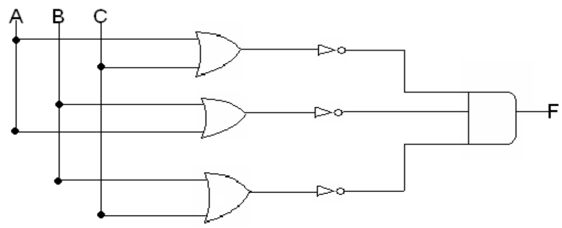
(d) Reduce the following Boolean expression using K – Map :

F(P, Q, R, S,) = Π (0,3,5,6,7,11,12,15) 3

2006 Delhi:

6. (a) State and verify Distributive Law. 2

(b) Write the equivalent expression for the following Logic Circuit : 2



(c) Express P +Q'R in canonical SOP form.. 1

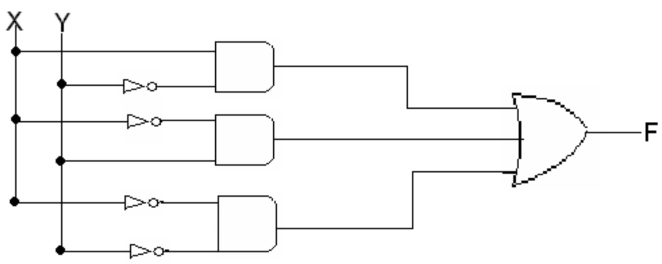
(d) Reduce the following Boolean expression using K – Map : 3

F(P, Q, R, S,) = ∑(0,3,5,6,7,11,12,15)

2005 Outside Delhi

6. (a) State and verify Absorption Law in Boolean algebra. 2

(b) Write the equivalent expression for the following Logic Circuit : 2



(c) Write the POS form of a Boolean Function F, Which is represented by the following truth table:1

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

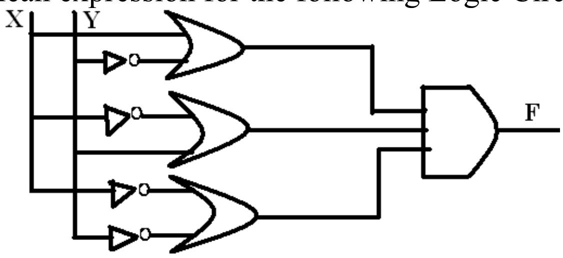
(d) Reduce the following Boolean expression using K – Map : 3

F(A, B, C, D,) = ∑(0,1,2,3,4,5,10,11,15)

<u>2005 Delhi:</u>

6.(a) State and verify Associative law in Boolean Algebra. 2

(b) Write the equivalent Boolean expression for the following Logic Circuit: 2



(c) Write the SOP form of a Boolean Function F, Which is represented by the following truth table:1

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(d) Reduce the following Boolean expression using K – Map : 3

F(A, B, C, D,) = Π (0,1,2,3,4,5,10,11,15)

<u>2004:</u>

6.(a) State and prove the Absorption law algebraically.

(b) Give the following truth table, derive a sum of product (SOP) and Product of Sum (POS) Form of Boolean expression from it:

A	B	C	F(A,B,C)
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(c) Obtain a simplified form for the following Boolean Expression using Karnaugh Map:

F(a,b,c,d) = ∑(0,1,2,4,5,7,8,9,10,11,14)

(d) Draw the logic circuit for a Half Adder using NAND gates Only. **(Out of Syllabus now)**

2003:

6. (a) State De Morgan’s Laws. Verify one of the De Morgan’s Laws using a truth table.
   (b) Verify X.Y’Z+X.Y’Z’+X’.Y’Z = X.Y’ + Y’.Z algebraically.
   (c) Write the dual of the Boolean Expression: (B’+C).A
   (d) Obtain a simplified form for a Boolean Expression:

   $F(U,V,W,Z,) = \sum(0,2,3,4,7,9,10,13,14,15)$

   (e) Draw the logic circuit for a half adder. (**Out of Syllabus now)**

2002:

6. (a) State the Distributive law and verify the law using Truth table. 1
   (b) Prove XY + YZ + Y’Z =XY + Z , algebraically. 2
   (c) Obtain the simplified form, of a Boolean expression using Karnaugh map. 2

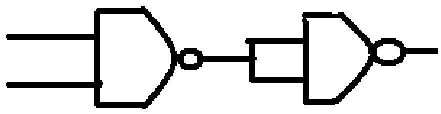
   $F(w,x,y,z)=\sum(2,3,6,10,11,14)$

   (d) Represent the Boolean expression (X+Y)(Y+Z)(X+Z) with help of NOR gates only. 1
   (e) Given the following truth table, write the product of sums form of the function.

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2001:

6. (a) State and verify Duality Principle.
   (b) Prove algebraically: x’y’z’ + x’y’z + x’yz’ + x.y’z = x’ + y’
   (c) If $F(a,b,c,d) = \Pi\ (0,1,3,4,5,7,8,9,11,12,13,15)$, Obtain the simplified form using K-map**.**
   (d) Seven inverters are cascaded one after another. What is the output if the input is 1?
   (e) Given the following circuit:



   What if the output if (i) both inputs are FALSE(0) (ii) one is FALSE and the other is TRUE.
   (f) Derive the expression for a Full a Adder.

2000:

6. (a)State Absorption Laws. Verify one of the Absorption Laws using a truth table.
   (b) Prove X’.Y+Y’.Z=X’.Y.Z+X’.Y’.Z’+X.Y’.Z+X’.Y’.Z algebraically.
   (c) Obtain simplified form for a boolean expression

   $F(x,y,z,w)= \sum$ (1,3,4,5,7,9,11,12,13,15) using Karnaugh Map.

   (d) Draw the logic circuit for a half adder.
   (e) Represent the Boolean expression X’Y+Y’Z with the help of NAND gates only.
   (f) Write the Sum of Products form of the function G(U,V,W) . Truthe table representation of G is as follows:

U	V	W	G
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

1999:

6.(a) State the distributive law. Verify the law using truth table.

(b) Prove x+x'y=x+y algebraically.

(c) Write the dual of the Boolean expression (x+y).(x'+y')

(d) Minimise F(w,x,y,z) using Karnaugh map.

F (w,x,y,z) = Σ (0,4,8,12)

(e) Draw the logic circuit for a half-adder. (**Out of syllabus now)**

(f) Represent the Boolean expression (x+y)(y+z)(z+x) with the help of NOR gates only.

Q 6 (g) Write sum of product form of the function F(x,y,z). The truth table representation for the function F is given below:

X	y	Z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

1998:

6 (a) State Demorgan's laws. Verify one of the Demorgan's laws using truth tables.

(b) Prove X+Y'Z=(X+Y'+Z')(X+Y'+Z)(X+Y+Z) algebraically.

(c) Write the dual of the Boolean expression (U+W)(V'U+W)

(d) Obtain a simplified form for a Boolean expression:F(U, V, W,Z) = Σ (0,1,3,5,7,9,10,11,12,13,14,15)

(e) Draw the logic circuit for a half-adder. (**Out of syllabus now)**

(f) Represent the Boolean expression X+Y.Z' with the help of NOR gates only.

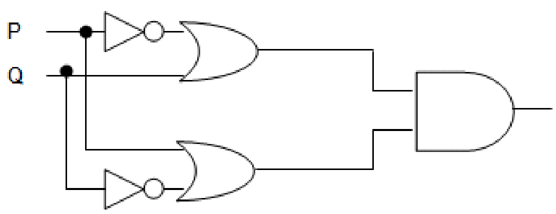
(g) Write the Product of Sum form of the function H(U,V,W), truth table representation of H is as follows:

U	V	W	H
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Model Paper 1:

6. (a) State and verify Demorgan's Laws. 2

(b) Write the equivalent Boolean Expression for the following Logic Circuit 2



(c) Write the POS form of a Boolean function F, which is represented in a truth table as follows:1

U	V	W	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

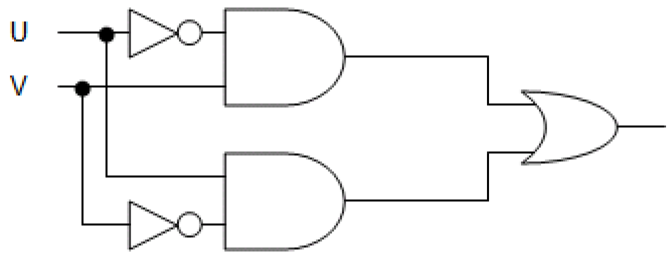
(d) Reduce the following Boolean Expression using K-Map: 3

F(A,B,C,D)=Σ(0,1,2,4,5,6,8,10)

<u>Model Paper 2:</u>

6. (a) State and algebraically verify Absorbtion Laws. 2

(b) Write the equivalent Boolean Expression for the following Logic Circuit 2



(c)Write the SOP form of a Boolean function G, which is represented in a truth table as follows:1

P	Q	R	G
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

(d) Reduce the following Boolean Expression using K-Map: 3

F(U,V,W,Z)=Π(0,1,2,4,5,6,8,10)

Other Important Paper:

6. (a) State and verify Distributive law in Boolean Algebra. 2

(b) Draw a logical circuit diagram for the following Boolean expression: A'.(B+C) 1

(c) Convert the following Boolean expression into its equivalent Canonical Sum of Product Form (SOP): (U'+V'+W').(U+V'+W').(U+V+W). 2

(d) Reduce the following Boolean Expression using K-Map: 3

F(A,B,C,D)=Σ(1,3,4,5,7,9,11,12,13,14)

ALL THE BEST